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AN N-GATE/N-SUBSTRATE OR P-GATE/P-SUBSTRATE CAPACITOR TO CHARACTERIZE POLYSILICON GATE DEPLETION EVALUATION

ABSTRACT OF THE DISCLOSURE

A capacitor structure for characterizing polysilicon gate depletion effects of a particular semiconductor fabrication process. In one embodiment, an N-Gate/N-Substrate capacitor is fabricated with the semiconductor fabrication process which is being evaluated for its polysilicon gate depletion effects. The N-gate of capacitor structure is driven to depletion while the N-substrate is simultaneously driven to accumulation. Capacitance-voltage measurements are taken. Based on these CV measurements, the polysilicon depletion effects are then obtained for that particular semiconductor fabrication process. In another embodiment, a P-Gate/P-Substrate capacitor is fabricated with the semiconductor fabrication process. The gate of the P-Gate/P-Substrate capacitor is driven to depletion while the substrate is simultaneously driven to accumulation. Based on the CV measurements performed on the P-Gate/P-Substrate capacitor, the polysilicon depletion effects can be obtained for that particular semiconductor fabrication process. In a third embodiment, a capacitor structure device is used to evaluate the polysilicon gate depletion effects of a semiconductor fabrication process. Different voltages are selectively applied to the gate of either an N-Gate/N-Substrate capacitor or a P-Gate/P-Substrate capacitor while its capacitance is measured. Based on the CV measurements, the polysilicon gate depletion effects for that particular semiconductor fabrication process is characterized.